A MIC X7 DHBT Frequency Multiplier With Low Spurious Harmonics

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ABSTRACT

We report on the design and measurement of a MIC X7 DHBT active frequency multiplier. The DHBT devices were fitted to a Gummel-Poon SPICE model which was then used with a harmonic balance analysis to simulate the active frequency multiplier. An edge-coupled filter was implemented for selective amplification of the desired harmonic, and results in 30 dB rejection of spurious harmonics. The X7 active multiplier design demonstrates output powers in the range of 0-4 dBm for moderate input signals (4-8 dBm).

I. INTRODUCTION

Frequency multipliers provide a convenient means for converting a very stable low-frequency oscillator source to higher frequencies for LO applications. Passive devices such as Schottky diodes or step-recovery diodes can be used, but require high input powers (> 15 dBm) and typically have high conversion losses, resulting in the need for both pre-amplification and post-amplification. On the other hand, active frequency multipliers require small input powers (-2 dBm to 6 dBm) and have high conversion efficiencies, and in some cases, even have conversion gain. Active frequency multipliers are already used throughout the satellite industry at frequencies below 5 GHz. However, these designs usually use conventional BJT devices and are constrained to operate at less than 5 GHz due to the low f_T of the devices. For operation at higher frequencies, it is necessary to use a higher frequency bipolar device, such as a double-heterojunction BJT (DHBT). At high frequencies, the distributed effects become important and it is necessary to develop a technique to model first the DHBT, and then simulate the active frequency multiplier. In this paper, we present the simulation, design, and measurement of a X7 DHBT active frequency multiplier implemented in microstrip technology.

II. DHBT MODELING

In order to do a nonlinear simulation of an active multiplier, it is first necessary to have a large-signal model of the device. A large-signal model of a device should have the ability to predict the DC I-V curves of the device, as well as the S-parameters at any given DC bias point. A commonly used model for a BJT in SPICE simulators and nonlinear simulators such as LIBRA is the Gummel-Poon model (see [1]). A deficiency of the Gummel-Poon model when applied to an HBT is the inaccurate modeling of the forward capacitances; nevertheless, this model has been used successfully for modeling HBT devices which are not operating near their f_T [2]. Also, the active multiplier simulation (next section) is not sensitive to small variations in the Gummel-Poon model parameters.

For this project, double-heterojunction bipolar (DHBT) devices were obtained from Hughes Research Labs in Malibu. These devices offer a higher collector-emitter breakdown voltage (> 8V) than a single heterojunction device and are therefore more suitable for frequency multiplier applications. The DHBT has a measured f_T of approximately 40 GHz, and an S21 greater than 5 dB up to 27 GHz.

The procedure for deriving the values of the Gummel-Poon model first involves taking the DC data (Gummel plot, fly-back method for emitter resistance, ...) and extracting all possible DC parameters (see [1] for more detail). Then, small-signal S-parameters are

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measured at various DC bias points, and the remaining unknown RF parameters are tweaked until a best fit is achieved between the measured and model-generated S-parameters. The critical RF parameters that determine the f_T of a device are the junction capacitances and the transit time. Table I lists the key parameters extracted from the DHBT measurements.

Model Parameter	Value
IS	6.8×10^{-14} A
NF	1.0
ISE	2.8×10^{-14} A
NE	1.16
ISC	2.8×10^{-14} A
NC	1.16
RE	0.4 Ω
RB	17.0 Ω
RC	0.4 Ω
TF	.70 ps
CJE	.91 pF
MJE	.42
CJC	.91 pF
MJC	.42

Table I: Gummel-Poon model parameters for the DHBT

III. ACTIVE MULTIPLIER DESIGN

An active multiplier can be modeled in a simple way if one considers the large signal model of a bipolar device (see Fig. 1). In this case, the input waveform is rectified at the base-emitter diode and this generates a spread of harmonic frequencies. After the harmonics have been generated, the current follower *selectively* amplifies the desired harmonic. The selective amplification is achieved through the use of a bandpass filter at the collector.

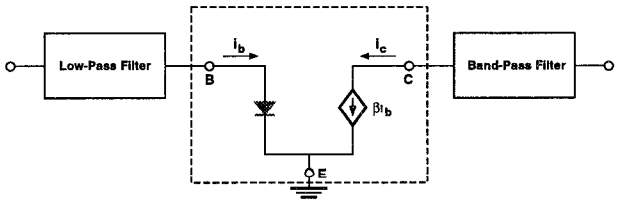

Fig. 1. Large signal model of a BJT.

The large signal model provides many insights into the operation of the active multiplier. For example, one can immediately find a good estimate of the maximum conversion efficiency. Page has shown that the maximum power conversion efficiency of a resistive diode multiplier is limited to $1/N^2$, where N is the harmonic number [3]. This means that a doubler is limited to 25% maximum efficiency, and a quadrupler to 6.25% maximum efficiency. To achieve this efficiency, a low-pass filter is placed at the input port to reduce the leakage of the desired higher harmonic frequency at the input port. The low-pass filter is also used for impedance matching for maximum input power. The harmonic frequency generated at the diode is then multiplied by the gain of the bipolar device. For an approximate value of gain, the measured S21 of the device at the output frequency could be used (note that this value assumes 50 Ω impedances, and could actually be somewhat higher if optimized for the particular circuit impedances). Thus, the maximum conversion efficiency is:

$$\text{Max. Conversion Eff.} \approx \frac{1}{N^2} * \text{S21(at output frequency)} \quad (1)$$

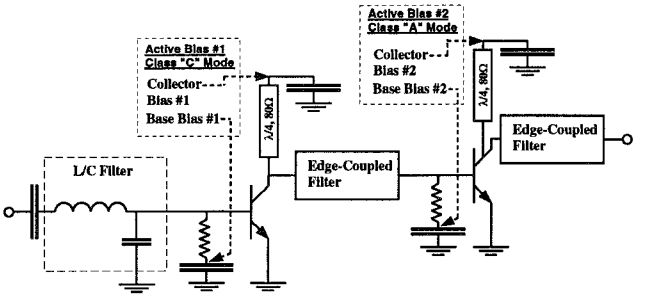

Fig. 2. Equivalent circuit of the active multiplier.

Nonlinear simulations were performed using EESOFF LIBRA software [4], and the equivalent microwave circuit of the X7 DHBT active multiplier is shown in Figure 2. Initial simulations show output powers of a single stage X7 DHBT multiplier to be in the range of -20 dBm to -10 dBm for input powers of 0 dBm to 5 dBm. The output power is low due to the very high harmonic number (X7). This power would not be high enough to drive any additional circuitry, and therefore a second DHBT stage was added to provide amplification of the multiplied signal from the first DHBT stage. This was accomplished by setting the bias of the second stage to class A mode. Figure 3 presents the simulated performance on LIBRA of the X7 DHBT active multiplier, and shows 0 dBm of power at 7 GHz for an input power of 4 dBm. Note that there is good suppression (> 30 dB) of all spurious harmonics. This was achieved using a two-stage

edge-coupled filter design. An advantage of an edge-coupled design is that it is a geometrically resonant filter (utilizing a $\lambda/4$ geometry), and therefore its general bandpass properties will be the same regardless of what input and output impedances are presented to it. This is not true of a lumped-element filter. Oscillations are prevented in the multipier design by utilizing resistive loading at the input of each DHBT.

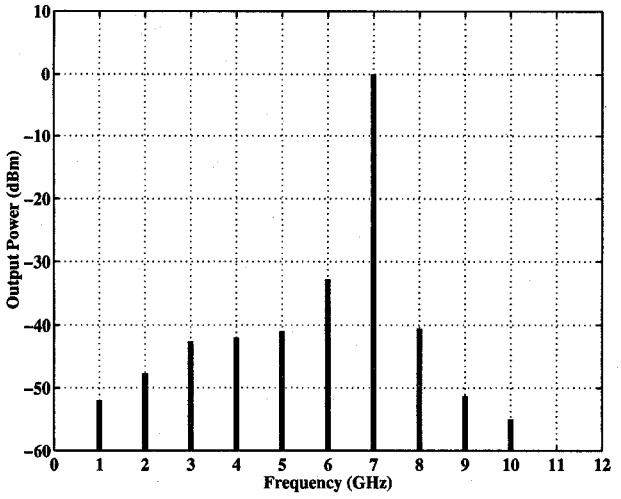

Fig. 3. Simulated performance on LIBRA with Pin = 5 dBm.

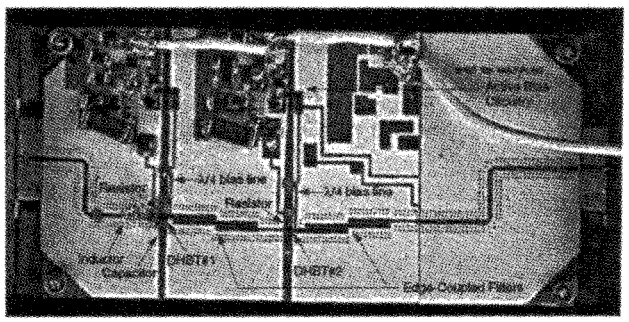

Fig. 4. Photograph of DHBT X7 active multiplier.

IV. MEASUREMENTS

The X7 DHBT active multiplier was fabricated on an ϵ_r=9.8, 0.38 mm thick Alumina substrate for an input frequency of 1 GHz and is shown in Figure 4. The DHBT devices were mounted on rails between sections of alumina substrates and the base and collector terminals were wire-bonded to the input and output microstrip lines, respectively, while the emitter was grounded to the rail. Active bias circuitry is provided by a conventional PNP transistor which sets the base and collector voltages. The base is connected via a resistor to a high-value capacitor which acts as an RF short for wideband resistive loading to prevent oscillations, as well as providing a connection point for the base bias. The collector bias is supplied via a $\lambda/4$ (at 7 GHz) high impedance transmission line terminated with a high-value capacitor, which should present an RF open at the collector. A DC blocking capacitor was placed at the input of the circuit; no DC blocks were needed elsewhere due to the inherent DC blocking of the edge-coupled filters. The circuit was then gap-welded to K-connector endplates for testing.

The X7 DHBT active multiplier was operated at 5.0 V and 30.8 mA of current, with the first (multiplication) stage drawing only 2 mA. The second stage (gain stage) required about twice as much current as was designed for, and this was attributed to a shift in I-V curves due to the self-heating effect of the DHBT. Since the measured S-parameters at the higher current were nearly the same, this had little effect on the experimental results.

Initially, the circuit was tested without a low-pass filter at the input port. The output edge-coupled filter of the X7 multiplier circuit is designed for a bandpass of 7.00 GHz. In operation, the circuit actually exhibited a peak at 7.16 GHz, but with dielectric pucks the edge-coupled filter was tuned to exactly 7.00 GHz. Whenever a signal that has a harmonic multiple which is 7 GHz was presented at the input, a strong 7 GHz signal was present at the output, with all other harmonics suppressed by a minimum of 20 dB. The strongest outputs were achieved for X2 and X3 multiplication, with the signal gradually decreasing as the harmonic multiplication number increased.

After the initial verification of the circuit operation, a 20 nH inductor and 0.4 pF capacitor were added in series/parallel at the input port of the active multiplier. Initially the LIBRA simulations indicated that these values should maximize the output power with a 1 GHz input (later a better match was found with a 25nH inductor and 0.9 pF capacitor, but was not tested). The output power did in fact increase with the addition of the input filter. The output spectrum is shown in Figure 5 and the spurious harmonics are 30 dB lower than the 7 GHz output signal. The measured output spectrum agrees well with the predicted values of spurious harmonics (Fig. 3). A power sweep at 1 GHz input is shown in Figure 6. It is seen that the multiplier operates for very low input power levels, and saturates at an output power of 4 dBm. Figure 7 shows the performance of the multiplier as the input frequency is changed about 1 GHz. An interesting

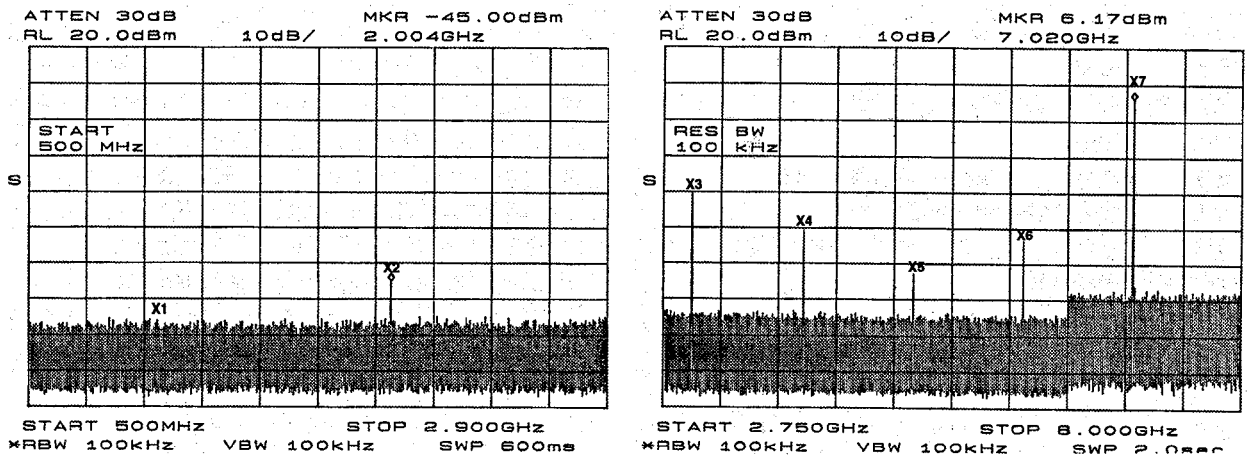

Fig. 5. Output spectrum with 1 GHz input.

discovery was that the multiplier circuit is quite narrowband, much more than would be expected from a two-section edge-coupled filter.

V. CONCLUSION

A X7 DHBT active multiplier was designed and tested for an output frequency of 7 GHz. It demonstrated output powers in the range of 0-4 dBm for moderate input signals (4-8 dBm). The circuit demonstrated excellent suppression of spurious harmonics (> 30 dB). The performance of the active multiplier circuit shows its feasibility for the replacement of passive multipliers in LO chains.

VI. ACKNOWLEDGMENT

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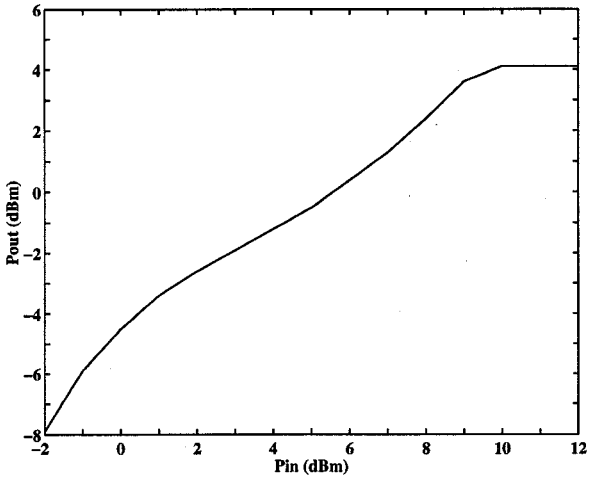

Fig. 6. Power sweep at 1 GHz.

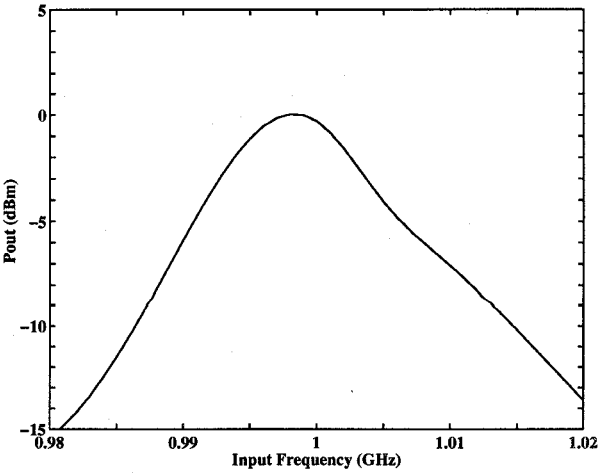

Fig. 7. Frequency sweep with Pin = 5 dBm.